REMARKS

Claims 1, 2, 4-6, 8, 15, 16 and18 are pending. Claims 7 and 17 are being cancelled without prejudice or disclaimer of the subject matter recited therein. Claims 1 and 4 are being amended by incorporation of the features of cancelled Claims 7 and 17 therein, respectively. No new matter is being added.

In section 3 of the Office Action, Claims 1, 2, 4, 5 and 15 are rejected under 35 USC § 102(b) as being anticipated by US Patent No. 6,556,1858. Applicants believe this to be a typographical error as the Office Action refers to the Applicant as Steensgaard-Madsen and this is corroborated by the Notice of References Cited at the end of the Office Action. It is therefore assumed that US Patent No. 6,271,782 (hereinafter referred to as the "Steensgaard-Madsen patent") is being cited on the above-mentioned grounds. Applicants are traversing this rejection.

The application includes two independent claims, namely Claims 1 and 4. Below, Applicants explain that the Steengaard-Madsen patent does not disclose all of the elements of Claims 1 and 4.

The Steensgaard-Madsen patent teaches a continuous-time sigma delta converter (col. 18, lines 3 and 4) that comprises a coarse quantiser 228 (a 5-bit sigma-delta modulator) coupled to a main quantiser 234 for providing a finer-grain quantization. As explained at col. 18, lines 9 – 23, an output signal (a first digital estimate) $d_0(k)$ is fed back to a summation unit via a primary feedback DAC 232, resulting in an output signal of the primary feedback DAC 232. An input signal g(t) is also provided and is typically expected to be small. The output signal of the primary feedback DAC 232 is subtracted from the input signal g(t). An analog residue signal $r_0(t)$ (col. 18, lines 24 and 24) results and is provided to the main quantiser 234 to yield an output signal $d_1(k)$ of the main quantiser 234. The residue signal $r_0(t)$ is usually very small and represents a quantization error. The output signal $d_1(k)$ is a digital error signal corresponding to the residue signal $r_0(t)$.

As explained at col. 21, lines 44-62, Fig. 27 shows the dynamic-range performance of a loop quantiser 236 of the main quantiser 234. In this respect, the Steensgaard-Madsen patent recognizes that the input signal g(t) can occasionally grow so as to constitute a large input signal, for example when the circuit starts-up. If nothing is done to respond properly to such large input signals, the main quantizer becomes unstable (col. 21, lines 55 – 57). Consequently, the step size of the loop quantiser 236 shown in Fig. 27 is small in the "midrange" in order for quantization-

noise performance to be "good" for small input signals g(t), but the step size increases near boundaries of the resolving range of the loop quantiser 236 in order to maintain stability of the main quantiser 234 in response to large input signals leaking through the loop quantiser 236. Furthermore, the Steensgaard-Madsen patent does not recognize the existence of non-ideal characteristics that include asymmetrical errors associated with non-ideal rising and falling edges of signal transitions. The Steensgaard-Madsen patent is very silent on this point. The non-ideality for which compensation is being made is the possible presence of large input signals.

Claim 1 recites a continuous-time sigma delta converter that comprises, *inter alia*, conversion means and a compensation circuit comprising error modeling components arranged to substantially model the non-ideal characteristics of the conversion means in order to provide a compensation signal, the non-ideal characteristics including asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

The Steensgaard-Madsen patent does not teach the modeling of non-ideal characteristics to provide a compensation signal, where the non-ideal characteristics being modeled include asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter, as recited in Claim 1. The Steensgaard-Madsen patent is silent in relation to the modeling of non-ideal characteristics when the non-ideal characteristics being modeled **include** asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter. In contrast, the Steensgaard-Madsen patent compensates for the possibility of large input signals being applied to the loop quantiser 236. The Steensgaard-Madsen patent does not teach compensation in the form of a compensation signal for the asymmetrical errors associated with non-ideal rising and falling edges of signal transitions.

In section 4 of the Office Action, Claims 6, 7, 16 and 17 are also rejected under 35 USC § 102(a) as anticipated over Handel et al. as "applied to Claims 1 and 4 above" and in view of Applicant Admitted Prior Art (AAPA). Again, the Applicant assumes that the reference to Handel et al. is a typographical error and that a reference to the Steensgaard-Madsen document was intended. It is therefore assumed that, in the Office Action, the non-idealities of the feedback path (errors associated with rising/falling edges signals) are considered to be implicitly disclosed by the Steengaard-Madsen patent.

As mentioned above in support of Claim 1, Claim 1 relates to a continuous-time sigma delta converter comprising, *inter alia*, conversion means and a compensation circuit comprising error modeling components arranged to substantially **model** the non-ideal characteristics of the conversion means in order to provide a compensation signal, the non-ideal characteristics

including asymmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter.

The Steensgaard-Madsen patent, even with the implicit teaching of the AAPA asserted in the Office Action, does not teach a continuous-time sigma delta converter that substantially **models** the non-ideal characteristics of the conversion means, where the non-ideal characteristics include asymmetrical errors associated with non-ideal rising and falling edges of signal transmissions of the converter, as recited in Claim 1. Even if the Steengaard-Madsen patent is construed to comprise signals that have non-ideal characteristics including asymmetrical errors of the type discussed above, the Steensgaard-Madsen patent still fails to teach:

(a) modeling of non-ideal characteristics that including these asymmetrical errors; and

(b) compensation for this particular type of non-ideal characteristic that includes asymmetrical errors associated with non-ideal rising and falling edges of signal transitions.

In view of the reasoning provided above, Applicants submit that the Steengaard-Madsen patent does not anticipate Claim 1, either alone or with the inclusion of the implicit teaching asserted in the Office Action that is provided by the AAPA.

Claims 2, 5, 6 and 8 depend from Claim 1. By virtue of this dependence, Claims 2, 5, 6 and 8 are also novel over the Steengaard-Madsen patent either alone or with the alleged implicit teaching of the AAPA.

Claim 4 provides for a method of compensation for known non-ideal characteristics in a continuous-time sigma delta converter. As explained above in support of Claim 1, the Steengaard-Madsen patent, with or without the alleged implicit teaching of the AAPA, does not disclose the feature of **modeling** the non-ideal characteristics of the conversion means in order to provide a compensation signal, where the non-ideal characteristics include asymmetrical error associated with non-ideal rising and falling edges of signal transitions of the converter, as recited in Claim 4.

In view of the reasoning provided above, Applicants submit that the Steengaard-Madsen patent, either alone or with the inclusion of the alleged implicit teachings of the AAPA, does not anticipate Claim 4.

Claims 15, 16 and 18 depend from Claim 4. By virtue of this dependence, Claims 15, 16 and 18 are also novel over the Steengaard-Madsen patent either alone or with the alleged implicit teaching of the AAPA.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

By: _____

David G. Dolezal
Attorney of Record
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125